What is claimed is:

1. A processor for processing variable length data including a plurality of arithmetic and logic units for processing data for every bit in a word unit, provided with:

a processing mask control unit for designating bits for dividing the data in each word to data to be processed and other data not to be processed and

an output select unit for selectively validating the function of processing by an arithmetic and logic unit in correspondence with the related bits for the above data to be processed and fetching results of the processing according to the above designation of bits by the processing mask control unit and the function of passing the data not to be processed through an arithmetic and logic unit in correspondence with the related bits.

2. A processor for processing variable length data as set forth in claim 1, wherein said processing mask control unit has a processing mask register for storing a logic 1 or 0 for designating whether each bit in said each word is a bit to be processed or a bit not to be processed in correspondence with each bit.

3. A processor for processing variable length data as set forth in claim 2, wherein said output select unit is comprised of output selectors receiving as input both the result of processing from said arithmetic and logic unit and said data not to be processed passed through the arithmetic and logic unit, in correspondence with each bit, selecting one of the above result and the above data, and outputting the selected one and where each output selector performs the selection according to said logic 1 or 0 from said processing mask register.

4. A processor for processing variable length data including a plurality of arithmetic and logic units for processing data for every bit in a word unit, provided

with:

a carry mask control unit for designating carry propagation for setting whether or not the carry produced from one arithmetic and logic unit is to be propagated to the other arithmetic and logic unit between adjoining arithmetic and logic units in correspondence with each bit and

a carry select unit for selectively validating a function of propagating a carry from one arithmetic and logic unit to the other arithmetic and logic unit according to said carry propagation designation by said carry mask control unit and a function of giving a fixed logic determined in advance as the carry to the other arithmetic and logic unit.

5. A processor for processing variable length data as set forth in claim 4, wherein said carry mask control unit has a carry mask register for storing a logic 1 or 0 for designating whether to propagate said carry or to give said fixed logic in correspondence with each bit.

6. A processor for processing variable length data as set forth in claim 4, wherein said carry select unit performs the selection by adding a function of selecting a carry from a memory device for storing carries produced by past processing as said carries from said one arithmetic and logic unit as well.

7. A processor for processing variable length data as set forth in claim 5, wherein said carry select unit is comprised of carry selectors receiving as input both of said carry from said arithmetic and logic unit and said fixed logic, in correspondence with each bit, and selecting one of the above carry and the above fixed logic and outputting the selected one and where each carry selector performs the selection according to said logic 1 or 0 from said carry mask register.

8. A processor for processing variable length data including a plurality of arithmetic and logic units for processing data for every bit in a word unit, provided

with:

a carry distribution unit for propagating a carry produced from one arithmetic and logic unit to other arithmetic and logic unit between arithmetic and logic units.

9. A processor for processing variable length data as set forth in claim 8, wherein said carry distribution unit is comprised of carry selectors receiving as input carries produced from said arithmetic and logic units in correspondence with each bit, selecting one carry determined in advance, and propagating the same to the arithmetic and logic units in correspondence with each bit.

10. A processor for processing variable length data as set forth in claim 9, further provided with a carry distribution setting unit for determining in advance from which arithmetic and logic unit the carry produced is to be selected for each said carry selector and designating the same.

11. A processor for processing variable length data including a plurality of arithmetic and logic units for processing data for every bit in a word unit, provided with

a first register for once storing data to be processed in a first word to be input to each arithmetic and logic unit,

a second register for once storing data to be processed in a second word to be input to each arithmetic and logic unit, and

a bit switch unit for simultaneously switching bits among multiple bits with each other while aligning bit locations for the data stored in the first and second registers.

12. A processor for processing variable length data comprised by connecting in parallel a plurality of subprocessors, each containing a plurality of arithmetic and logic units having identical configurations and

processing data for every bit in a word unit, wherein each subprocessor is provided with:

a carry I/O interface unit which becomes effective when a length of said data to be processed exceeds the bit length of said one word, propagates the carry produced from an arithmetic and logic unit in one of two adjoining said subprocessors to an arithmetic and logic unit in the other subprocessor and propagates the carry produced from the arithmetic and logic unit in said other subprocessor to the arithmetic and logic unit in said one subprocessor.

13. A processor for processing variable length data as set forth in claim 12, wherein each carry I/O interface unit has a carry selector receiving as input the carry produced from each arithmetic and logic unit and the carry produced from any arithmetic and logic unit in adjoining subprocessors in correspondence with each bit, selecting one carry determined in advance and propagating this to the arithmetic and logic unit corresponding to each bit and transferring the selected carry to said adjoining subprocessor.

14. A processor for processing variable length data as set forth in claim 13, wherein each said carry I/O interface unit further has a transfer carry control unit having transfer carry selectors each receiving as input a selected carry selected by said carry selector and selecting a transfer carry to be transferred to said adjoining subprocessor in correspondence with each bit and giving a select indication determined in advance with respect to each said carry selector.

15. A processor for processing variable length data comprised by connecting in parallel a plurality of subprocessors, each containing a plurality of arithmetic and logic units having identical configurations and processing the data for every bit in a word unit, provided with:

a scheduler functioning when the length of

said data to be processed exceeds the bit length of said one word, allocating data to said plurality of subprocessors for distributed processing, and controlling the processing at the subprocessors to which the data is allocated.

16. A processor for processing variable length data as set forth in claim 15, wherein said scheduler makes the other subprocessor use the related arithmetic and logic unit when one or more of said arithmetic and logic units in one subprocessor become idle.